A primer on 3D-IC design challenges

Know the 3D-IC design challenges such as system exploration, floorplanning, analysis, and design for test (DFT), and learn how designs will evolve as 3D-IC goes on to become a necessity for managing power, performance, form factor, and cost goals.

By Samta Bansal
Senior Product Marketing Manager
Cadence Design Systems

Last October 2010, Xilinx announced its use of a 2.5D through-silicon via (TSV) process for their Virtex-7 FPGAs. This was followed by announcements from TSMC, Samsung, Nokia, Micron, and Elpida about using 3D-ICs with TSVs, showing that TSV technology has emerged as a proven and viable technology that offers compelling advantages in power, performance, form factor, and time to market. By making it possible to stack analog, digital, logic, and memory dies at different process nodes, 3D-ICs offer what may be the best alternative to the skyrocketing costs of advanced process nodes.

This article examines the terminology associated with 3D-ICs and reviews what 2.5D is, what 3D is, and what the tradeoffs are. It then introduces some 3D-IC design challenges such as system exploration, floorplanning, analysis, and design for test (DFT), and shows how designs will evolve as 3D-IC goes on to become a necessity for managing power, performance, form factor, and cost goals.

3D-ICs with TSVs

Despite the recent buzz in the industry about 3D technology, the concept of 3D is not so new at all. 3D packaging has been around for years—stacks of die with wirebonds, package-in-package (PiP) design, and package-on-package (PoP) design, to name a few. PoP is a widespread configuration that combines a stack of memories on top of an application processor or digital baseband. Both PiP and PoP assemblies may be categorized as 3D-ICs, but neither offers the performance, power, density, and form factor of true 3D-ICs using TSVs. What is new is the extension of the 3D package concept into the IC side.

One extension is to add a silicon interposer substrate (either passive or active) to provide much finer die-to-die interconnections, thereby increasing performance and reducing power consumption. A silicon interposer includes TSVs, which are vertical electrical connections passing through a silicon die, connecting the upper metal layers to additional back-side metal layers (figure 1). This technique is often referred to as “2.5D” packaging.

![Figure 1: 2.5D design involves adding a silicon interposer with TSVs (only two die are shown for simplicity).](image-url)
A “true” 3D-IC using TSVs involves two or more die connected together using TSVs. For example, consider a scenario in which one die containing TSVs is attached to the system-in-package (SiP) substrate using conventional flip-chip technology. Meanwhile, a second die is attached to the first (figure 2). The 3D-IC shown above is referred to as a back-to-face (B2F) configuration, because the back of the first die is attached to the face of the second die. It is also possible to have back-to-back (B2B) and face-to-face (F2F) configurations, especially when more than two die are stacked in this manner.

**Figure 2:** A simple 3D-IC using TSVs.

Except for memory stacks, it is unusual these days to see more than two layers of dice stacked on top of each other. However, the potential of 3D-IC design is huge and once the technology is mainstream, it will be possible to build complex scenarios (figure 3).

**Figure 3:** A more complex 3D-IC using TSVs and six dice.

Compared to a wire-bonded SiP (3D package), TSVs offer reduced RLC parasitics, better performance, more power savings, and a denser implementation. Compared to a silicon interposer (2.5D) approach, a vertical “true” 3D die stack offers a higher level of integration, smaller form factor, and a faster design cycle. But a 3D stack raises some additional challenges—including thermal, timing, and power management concerns—which are mitigated in the 2.5D approach. So, deciding between 2.5D and 3D requires making a tradeoff among power, performance, form factor, and cost. It also depends on the applications you are targeting. FPGAs, CPUs, GPUs, gaming, and servers are better suited for 2.5D; low-power applications like smart phones and other wireless applications are better suited for 3D.

**Challenges, requirements**

While 3D-ICs with TSVs do not require a revolutionary new 3D design system, they do require some new capabilities that need to be added to existing toolsets for digital design, analog/custom design, and IC/package co-design. 3D-ICs require additional components to enable the 3D interconnection (figure 4).
1. Redistribution layers (RDLs) are typically formed on the back side of the die. Bumps can thus be placed on both the front side and the back side.
2. TSVs can be drilled between the first metal layer and the back-side RDL. TSVs may have diameters from 1 to 5 microns.
3. “Micro-bumps” (much smaller flip-chip bumps) have to be aligned to create a data path from one die to another.

Figure 4: Unlike regular chips with flip-chip bumps (left), 3D-IC die can have micro-bumps on both sides of the die (right).

To provide 3D-IC support for EDA tools, these additional components must be understood and accounted for. Since many 3D stacks combine digital and analog/RF circuitry, a strong analog/mixed-signal capability plus a robust IC/package co-design capability and PCB layout system are critical for providing a “complete” 3D-IC realization methodology. Without an integrated approach to 3D-IC design, optimizing system cost with the shortest possible turnaround time will be challenging. 3D-IC design should be a shared effort among system architects, package designers, IC designers of various dies (which probably come from different places/vendors), PCB designers, and design for test (DFT) engineers: and that calls for a system that can handle the handshake between different platforms, close collaboration between different design environments, and co-design among groups that have historically worked separately.

In addition, new capabilities such as the following will be needed to meet 3D-IC design challenges:
- System-level exploration
- 3D floorplanning
- 3D implementation (placement, optimization, routing)
- 3D extraction and analysis
- 3D design for test (DFT)

System-level exploration 3D-IC TSV technology is a convergence of silicon and packaging with the design, making it possible to conceive and design new architectures. To fully benefit from 3D-IC TSVs and make this technology cost-effective, different 3D architectures need to be considered and evaluated at a very early stage. Existing system-level exploration tools can provide early power, area, and cost estimates, and they allow what-if explorations across architectures, silicon IP choices, and foundry processes. However, these tools need to be extended to serve stacked die implementations, package, and manufacturing considerations, as well as to provide some guidance on tradeoffs that system houses would have to make among cost, power, and performance.

Figure 5: Planning, implementing, and verifying 3D-ICs in a Cadence environment.
3D floorplanning

3D floorplanning is complex enough in today's giga-scale designs. Adding a third dimension makes floorplanning even more challenging. Since TSVs can be very large compared to logic gates (they add more wire length and extra coupling, which is mitigated by keep-out zones that add area) a TSV-aware 3D floorplanner must allocate optimized TSV resources with respect to logic gates.

Additionally, TSV-aware 3D floorplanning must provide an abstraction level that can capture all the dice, and provide a unified representation of intent for placement and routing tools. A 3D floorplanner should work in the X, Y, and Z directions, and should have visibility into the top and bottom of each die. This helps optimize the placement of blocks, TSVs, and micro-bumps, and it shortens interconnect distances, thus improving performance and power. Ideally, a 3D floorplan has to be thermal-aware to avoid thermal hotspots and take mechanical stress into consideration. Thermal awareness will also help users determine the optimal placement of die into stacks.

3D implementation

Synthesis, placement, and routing for 3D-ICs brings forth a number of new considerations. For example, there are new layout rules that may be driven by features on adjacent die. The back-side redistribution layer (RDL) is a new layout layer. And given their size, TSVs themselves are a significant new layout feature. An implementation system that supports 3D-ICs must be made "double-sided aware," taking into account both the top and bottom of each die. This may call for a new modeling and database infrastructure, TSV-specific tools, and support for a variety of stacking styles.

With 3D-IC placement, optimization, and routing, it is important to build power, clock, and thermal considerations into the implementation solution. Analog implementation environments also need to add support for 3D-ICs. Examples of useful capabilities include multichip visualization with background views; support for bump, TSV, and reverse-side routing; and connectivity extraction maintained through TSV connections.

Throughout the design convergence process, design intent must be maintained and checked, and the necessary abstraction techniques must be applied for proper implementation and analysis.

3D extraction and analysis

If extraction and analysis wasn’t challenging enough in a 32nm 2D scenario, design convergence will be even more complicated with 3D-ICs. Existing extraction and analysis tools must consider RLC parasitics for TSVs, micro-bumps, and interposer routing, and they must be made 3D-aware. Timing, signal integrity, power, and thermal gradients must be analyzed across multiple die and take packaging into consideration.

Signoff raises new questions with 3D-IC stacks. When is the right time to sign off, and what are the appropriate signoff points? Can design rule checking (DRC) and layout-versus-schematics (LVS) run on the entire stack? Should and can timing be verified for the entire stack? Is there any crosstalk between die? Finally, electromagnetic interference (EMI) is a potential concern for 3D–ICs and a consideration for the analysis tools.

3D DFT

Last but not least, design for test (DFT) for 3D-ICs is even more critical than for 2D ICs. While wire-bonded systems-in-package (SiPs) may have a few hundred interconnects, 3D-ICs may have thousands if not tens of thousands of interconnects. Even a single defective TSV can render an entire stack unusable. If individual TSVs have 99.9% yield, at least one defective TSV can be expected in a stack of 1,000 TSVs.

**Functional Design**
- z2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

**Existing Design-for-Test**
- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Stack product: IEEE Std 1149.1

**3D DFT Architecture**
- Test wrapper per die
  - Based on IEEE 1149.1 or 1500
  - Two entry/exit points per die:
    1. Pre-bond: extra probe pads
    2. Post-bond: extra TSVs

*Figure 6: The imec-Cadence implementation of a 3D-IC DFT architecture within the Cadence Encounter environment (source: imec).*
A sound test methodology for 3D-ICs is necessary for IC designers to have the confidence to design them and to enable per-bond, mid-bond, post-bond, and post-package (final) testing. Fortunately, solutions are starting to emerge (figure 6). 3D-IC testing can leverage a large body of technology and experience with modular SoC testing by using DFT wrappers and extending them to 3D testing. In the SoC world, modular testing is made possible by DFT wrappers such as the IEEE 1149.1 boundary scan standard and the IEEE 1500 embedded core test standard. For 3D-IC testing, these wrappers need to be enhanced with 3D-specific extensions such as the following:

- Additional probe pads for pre-bond testing
- Test “turnarounds” that start and finish the test access points at the bottom side of each die
- Test “elevators” that propagate test data vertically through the stack

To provide test generation, the wrappers should support both the internal testing of each die as well as all the inter-die interconnect logic and TSVs. In addition to the traditional fault models used for digital testing (stuck-at, transition, stuck-open, bridge faults), 3D-ICs require specific interconnect fault models to test the TSVs and micro-bumps. The test architecture described here was refined through collaboration between Cadence and the Belgian research institute imec.

**What this means for a designer**

In addition to expanding EDA tools to be 3D-aware, designers have to start thinking in 3D as well. For system architects, 3D-IC architectures open up a new world of possibilities. At the same time they also introduce a lot of moving parts that architects must be aware of while doing system planning. There are many considerations for deciding on the most optimized and cost-effective architecture. System architects must factor in new technical challenges and costs associated with the 3D-IC ecosystem to make it all work together.

If the life of IC designers was hard enough in 2D, 3D-ICs will not make it any easier. Designers need to understand the new technical challenges with 3D-ICs—thermal, test, crosstalk, etc.—and account for these in their individual die, but that alone is not sufficient. Before designers can sign off their die, they need to interact with whoever designed the die on top of their die, as well as the IC designer for the bottom die/package. Handoffs between the same company’s designers are difficult enough, and 3D-die handoffs could be between different companies or participants in the ecosystem.

EDA tools can help minimize some of those interactions by providing a common platform, yet the overall design task will get challenging where dies are coming from different places and are implemented in different environments. A proper handoff point must be agreed upon by the industry to make it easier for IC designers to exchange design data. In addition, designers need to expand their thinking to the system context. Knowing just their die and what it is supposed to do will not be sufficient. Having a complete picture and understanding of the system(s) their die can potentially go into will become one of the differentiating factors for their product.

**Conclusion**

3D-ICs with TSVs are an increasingly attractive option, and they need “3D-aware” design tool support. Isolated point tools won’t result in optimized, cost-effective solutions that take full advantage of the potential benefits of 3D-ICs. What's needed is a comprehensive end-to-end solution that serves digital, analog, and package design teams.