Low voltage differential signaling is a physical layer data interface standard defined by the TIA/EIA-644 and the IEEE 1596.3 standards. It is designed for high-speed, low-power and low-noise point-to-point communication, typically over balanced, controlled-impedance media of 100Ω. Like other differential signaling standards, LVDS radiates less noise than single-ended signals due to the canceling of magnetic fields, and is more immune to noise because it is coupled onto the two wires as a common-mode signal. In addition, LVDS drivers use a current-steering output configuration which reduces ground bounce and eliminates shoot-through current compared with voltage-mode drivers used in other differential signaling standards. Reduced voltage swing (only ±350mV vs. ±800mV for PECL and ±2V for RS422) allows LVDS to achieve data rates comparable to PECL (>800Mbit/s) while dissipating only one-tenth the power. This combination of high-speed, low-power and low-noise make LVDS ideal for applications such as telecom and networking equipment backplanes, 3G cellphone base station intra-rack connections and digital video interfaces. In addition to the benefits discussed, LVDS Serdes (Figure 1) will also contribute enormous space and cost savings to designs. This reduces interconnect by five times.

In communication and other apps with high card counts such as 3G systems, these products translate to an enormous savings in space and cost.

Using capacitors to AC-couple an LVDS data link provides many benefits, such as level shifting, removal of common-mode errors and protection against input-voltage fault conditions. This article helps designers select the proper capacitor and the termination topology for this design approach. Common troubleshooting issues are discussed.

LVDS logic inputs are one of many available logic standards. Using an AC-coupled link can offer the desired level translation, if the signal source provides sufficient amplitude for the LVDS inputs, which are typically 100mV_{p,p} differential. Figure 2 depicts a negative ECL logic source that converts the signal levels to LVDS logic through such an AC-coupled link.

Overvoltage protection

LVDS signals are always AC-coupled in automobile Serdes links. Protecting the car’s battery voltage from shorts is the primary motivation for this configuration. A universal requirement for any signal entering the wiring harness is that it must withstand a short-to-battery voltage without damage. With an AC-coupled LVDS link, there is only a brief

**INTERFACE ICs**

**Tap AC-coupling for LVDS signals**

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AC-coupled LVDS also allow the receiving IC to set its optimal common-mode voltage. In Figure 3, a typical LVDS input is shown, in this case the MAX9248. An internal reference voltage, often 1.2V, biases two high-impedance termination resistors.

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Figure 4: The termination topology can be selected from three primary circuits.

Figure 5: Shown is an AC-coupled LVDS link without DC-balance.

Capacitor selection
Several factors affect proper capacitor selection.
Value—The value of the AC-coupling capacitors used in the LVDS link depends on several parameters, including: output drive level, input threshold level, load impedance, cable length and longest pulse duration.

Consequently, the total attenuation from DC resistance, AC attenuation and capacitive coupling droop must be less than -8dB. The load impedance is usually a 100Ω differential on both ends. Analyzing the cable length requires that both the cable’s AC and DC attenuation, plus losses from connector resistance all be considered.

Finally, the data itself must be considered. The longest pulse that the LVDS link must transmit is a function of the operating frequency and the maximum number of consecutive 1s (or 0s) that the data protocol will pass.

If all these calculations are too involved for an application, simply choose 0.1µF capacitors, which will suffice for most applications. When the data rate drops below 10MHz or when longer cables lengths are used, then the required value should be verified, either by calculation, simulation or actual measurement.

Voltage and dielectric—The operating voltage of the capacitors should be greater than the expected peak voltage during a fault condition. In automotive applications, the peak fault voltage is 18V. Double-fault conditions such as double battery voltage or load dump usually do not need to be considered.

Use capacitors with X5R, X7R or equivalent dielectric specifications. Avoid dielectrics with temperature coefficients, such as Y5V or Z5U.

Termination configuration
The termination topology can be selected from three primary circuits: pure differential, center-tapped differential and Thevenin termination (Figure 4).

Pure differential is the most common termination topology, and works well for terminating signals in a well-shielded environment. The center-tapped differential termination splits the 100Ω termination into two 50Ω resistors, with a bypass capacitor at the center tap. This approach works well for noisy environments, as any common-mode energy induced on the LVDS pair sees a low impedance to ground. Both the pure differential and the center-tapped differential termination must be used with internally biased LVDS inputs.

If the LVDS receiver is not internally biased and if the input signal is AC-coupled, a Thevenin termination must be used. Select the resistors so that the Thevenin impedance on each line is 50Ω and that the Thevenin voltage on each line is 1.2V. The values in Figure 3 work for a 3.3V supply.

Troubleshooting
The data transmitted over an AC-coupled LVDS link must be DC-balanced, which means that the number of 0s transmitted must be as close as possible to the number of 1s transmitted. Clock signals

Figure 6: A fail-safe circuit identifies input faults; it disables the output driver if a fault is detected.
of nominally 50 percent duty cycle are intrinsically DC-balanced. Many data encoding algorithms, such as Manchester encoding, also provide DC-balanced data streams. **Figure 5** depicts the plot of a link without DC-balance.

The top traces in Figure 5 (red and blue) reflect the single-ended measurement of a 20 percent duty-cycle pulse stream. The bottom trace (green) is a differential measurement across both complementary and true signals. The differential measurement is not centered on 0V and is skewed. A careful analysis shows that the area under each half of the waveform is equal. The AC-coupled link is unable to transmit any DC current. For this case, the negative excursion is just below 100mV, violating the LVDS minimum input levels.

Some LVDS devices have a failsafe circuit on their inputs. A failsafe circuit identifies input faults and disables the output driver if a fault is detected. The MAX9180 low-noise LVDS repeater is an example of this design, and shown in **Figure 6**. If an AC-coupled LVDS link is attempted with a fail-safe circuit, a Thevenin termination of the inputs is required. If this configuration is not used, the DC voltage at the inputs is almost VCC, which is outside the common-mode voltage range for the LVDS device.