Evaluate clamping voltages for ESD protection

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Designers of handheld products such as cellphones, digital cameras, MP3 players and PDAs are constantly challenged to provide more functionality in smaller form factors while reducing the overall system cost. IC designers have eased this trend by improving the speed and performance of their devices while decreasing the size of silicon real estate. However, the reduced dimensions of IC features have resulted in devices that are more susceptible to damage from ESD voltage.

This trend can have a negative impact on the reliability of the end product and can increase the likelihood of field failures. As a result, designers of handheld products are challenged to find cost-effective ESD solutions that can clamp to lower voltage levels to maintain high reliability.

Common waveform

The most commonly used waveform for defining a typical ESD event at the system level is the IEC61000-4-2 waveform, which is distinguished by its sub-nanosecond rise time and high current levels (**Figure 1**). The spec for this waveform outlines four levels of ESD magnitude. Most designers are required to qualify their products to the highest level—8kV contact discharge or 15kV air discharge. When testing at the component level, the contact discharge test is more appropriate, since the air discharge test can't be performed on such small components.

An ESD protection device should reduce an ESD input of thousands of volts down to a safe voltage for the IC being protected and shunt current away from the IC. Although the input voltages and currents of the required ESD waveforms have not changed over the last few years, the minimum voltage level required to protect ICs has decreased. In the past, IC designs were more robust and could handle higher voltages, so it was sufficient to choose any protection diode that was capable of surviving the IEC61000-4-2 L4 requirements. With newer, more sensitive ICs, designers must not only ensure that the protection device is capable of surviving the IEC61000-4-2 L4 standard, but also make sure that the device will clamp the ESD pulse at a low enough voltage so that the IC is not damaged. When selecting the best protection device for a given application, designers must consider how low the ESD protection device clamps an incoming ESD event.

Choose effectively

Key DC specifications included in protection diode datasheets are breakdown voltage, leakage and capacitance. Most datasheets will also state a maximum rating for IEC61000-4-2, which indicates that the diode will not be damaged by an ESD pulse at the specified level. The problem with most datasheets is that they do not have any information about clamping voltage for high-frequency, high-current transients such as ESD. Clamping voltages of protection diodes are considerably higher during these types of transient events compared with the DC voltage specified on the datasheet. However, it is difficult to specify a clamping voltage for the IEC61000-4-2 spec because it was intended to be a pass/fail spec at the system level, and the frequency is very high. To apply this spec to a protection device, it is crucial to examine not only if the protection diode passes or fails, but also how low it clamps the ESD voltage.

The best way to compare the clamping voltages of protection diodes is to take an oscilloscope screenshot of the actual voltage waveform across the diode during an ESD event. When looking at a voltage waveform of an ESD protection device exposed to the IEC61000-4-2, there will typically be an initial voltage spike, followed by a secondary peak, after which the voltage will eventually level off. The initial spike is caused by a combination of the initial current spike of the IEC61000-4-2 waveform and an overshoot resulting from inductance in the testing structure. The initial spike duration is short, however, which limits the energy transferred to the IC. The protection device's clamping performance is best displayed in the curve following the initial overshoot. The secondary peak is of primary concern because the voltage waveform holds for a longer duration, increasing the total energy that the IC will be exposed to. Clamping voltage is defined as the maximum voltage of the secondary peak.

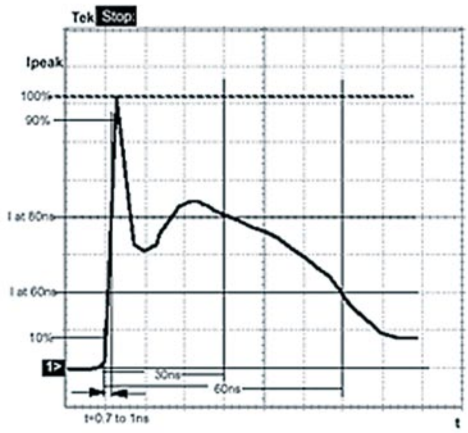
Benchmarking comparison

To do a fair comparison, the parts chosen should have similar package sizes and datasheet specifications. Consider three ESD protection diodes that are drop-in replacements for each other when comparing electrical characteristics from the datasheets.

Level ratings

Level	Total voltage (contact dischare) (kV)	Test voltage (air discharge) (kV)	First peak current (A)	Peak current at 30ns (A)	Peak current at 60ns (A)
1	2	2	7.5	4	2
2	4	4	15	8	4
3	6	8	22.5	12	6
4	8	15	30	16	8

(a)



(b)

Figure 1: The most commonly used waveform for defining a typical ESD event at the system level is the IEC61000-4-2 waveform, which is distinguished by its sub-nanosecond rise time and high current levels.

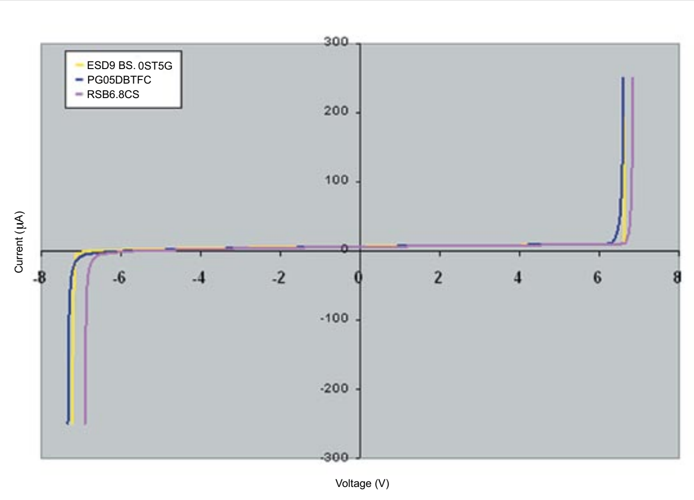


Figure 2: The DC performance of the ESD parts may look identical.

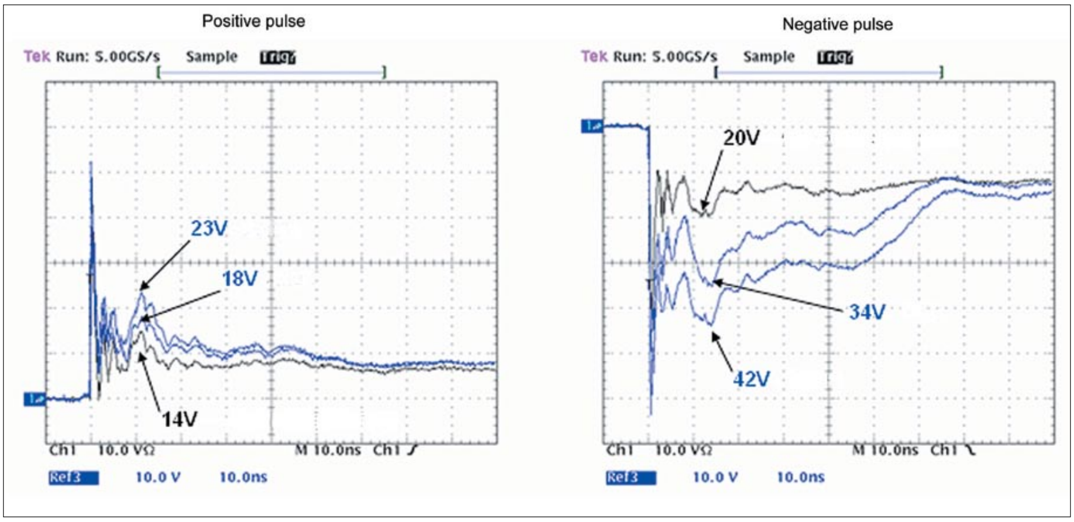


Figure 3: Voltage clamping comparison of ESD protection diodes shows that the protection solution with the black waveform offers lower clamping voltages for ESD pulses compared with the solutions with blue waveforms.

The devices are all bidirectional ESD protection diodes that have identical breakdown voltages (6.8V), capacitance (15pF) and package outlines (1mm x 0.6mm x 0.4mm). The products chosen for this study were the RSB6.8CS from Rohm Co. Ltd, the PG05DBTFC from Korea Electronics Co. Ltd and the ESD9B5.0ST5G from ON Semiconductor.

The DC performance of parts may look identical (**Figure 2**). In addition, these parts claim to be compliant with IEC61000-4-2 L4 standard, thus they will all survive an ESD strike of up to 8kV contact.

To compare the clamping performance of each device, take an oscilloscope screenshot of the voltage waveforms during an ESD event. **Figure 3** shows the response of each diode on the same graph for a positive and negative ESD pulse. The input pulse used was a standard IEC61000-4-2 L4 contact (8kV).

According to Figure 3, the protection solution with the black waveform offers lower clamping voltages for ESD pulses compared with the solutions with blue waveforms. For the positive pulse, the ESD9B5.0ST5G clamps at 14V, while the PG05DBTFC clamps at 18V and the RSB6.8CS clamps at 23V. The difference of the three devices becomes more evident during application of the negative pulse. The clamping voltages for the negative pulse were 20V for the ESD9B5.0ST5G, 34V for the PG05DBTFC and 42V for the RSB6.8CS.

The three devices perform differently during negative ESD events, where the PG05DBTFC has 70 percent greater and the RSB6.8CS has more than double the clamping voltage of the ESD9B5.0ST5G. The overall voltage for the negative pulse that gets through some products are potentially dangerous to new IC designs that are more susceptible to ESD damage. The ESD9B5.0ST5G, however, maintains low clamping voltage in both directions, minimizing the risk for both the positive and negative ESD pulses.

A good protection device needs to clamp well for both positive and negative ESD pulses to guarantee the highest reliability of products in real-world conditions. Low clamping voltage in both directions ensures that the device will protect the most sensitive ICs, which enables the designer to use the latest semiconductor technology that pushes the envelope for functionality and speed. Companies must design their protection devices not only to survive an ESD event, but also to provide the lowest clamping voltage available in the market. Manufacturers of ESD protection devices should include ESD clamping screenshots on the datasheets for all new products.