

# Test your products for PCIe compliance, interoperability

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Compliance Workshops, which include training sessions on the latest PCIe specifications and compliance testing for products, are the last of several steps in the PCI-SIG process for compliance and interoperability.

Building interoperable products requires a solid specification such as PCI-SIG interconnect specifications, which have been widely adopted in different markets in the last 15 years. Less obvious though are the test specifications generated by PCI-SIG workgroup members, which correspond directly to the interconnect specifications. Assertions from the test specifications yield test definitions, which begin the objective process of validating a component's compliance with the interconnect specification. When test specifications are determined, a series of hardware and software tools are created to apply the tests in a real-world environment. The tools are run against member-developed systems, add-in cards and silicon, and then carefully checked for correctness. Then, the test tools are approved for official use in determining product compliance and become

part of subsequent Compliance Workshops.

Up to four different major areas are tested at a PCIe Compliance Workshop. Three different dedicated hardware boards and several software tools are made available to PCI-SIG members to help them validate these areas (**Figure 1**).

**PHY layer**—All components are tested at their PHY layer, the electrical signalling at the heart of PCIe. For motherboards, the compliance load board (CLB) is used to connect an oscilloscope to PCIe slots with different width measurements. For add-in cards, the compliance base board (CBB) provides a corresponding connection. Data captured with the oscilloscope is run through software provided by PCI-SIG to analyze the eye pattern, jitter and bit-rate of the component (**Figure 2**). These tests verify that PCIe components have the correct transmitter eye diagram and signal amplitude required for interoperability.

**Link and transaction layers**—Components are also exercised at the packet level, with various errors injected and responses analyzed. Different protocol details and boundary conditions such as reserved fields, bad CRCs, duplicate packets and the like are also checked. The

protocol test card (PTC) in Figure 1 and its associated software provide this function for both motherboards and add-in cards.

**Configuration space**—Every PCI device has a special address space for configuration and control mechanisms. The PCIe Configuration Test Software tool analyzes and tests this aspect of each PCIe component. Specific register characteristics are checked, as well as any implemented optional features such as advanced error reporting and device serial number. Every component is checked to ensure it supports the required PCI power management functions.

**Platform BIOS testing**—PCIe motherboards undergo one more set of tests designed to validate that the system BIOS correctly configures and provisions PCIe components. The PTC and software are used here to emulate a more complex hierarchy of PCIe devices that can be physically plugged into the system being tested. Memory and I/O address space allocation is tested, along with provisioning and configuration of PCIe switches.

The specifications, procedures and tools listed are made available to and are used by PCI-SIG members in their own labs before bringing their products to a Compliance Workshop.

One aspect of the actual Compliance Workshop is very difficult and costly to reproduce elsewhere—the interoperability testing of PCI products with other member products. For example, at the last Compliance Workshop in Taipei, 16 systems and 90 add-in cards were presented. Moreover, the PCI-SIG provides several “Gold” systems that have been determined to be fully compliant and provide a good platform for add-in card testing.

Generally, testing at a Compliance Workshop focuses on systems. Each system has its own setup and has add-in cards rotating among them. Pre-registration for the event is essential so that PCI-SIG can create a schedule that maximizes the number of add-in cards and systems tested against one another. The PCI-SIG has run Compliance Workshops with over 24 systems and accommodated all necessary testing. This testing capacity is achieved due to the type of testing structure implemented in the Compliance Workshops. PCI-SIG “Gold” systems and add-in cards are also incorporated into the schedule, so every add-in card is guaranteed to test with each required “Gold” system and similarly, every system is guaranteed to test with each required “Gold” add-in card.

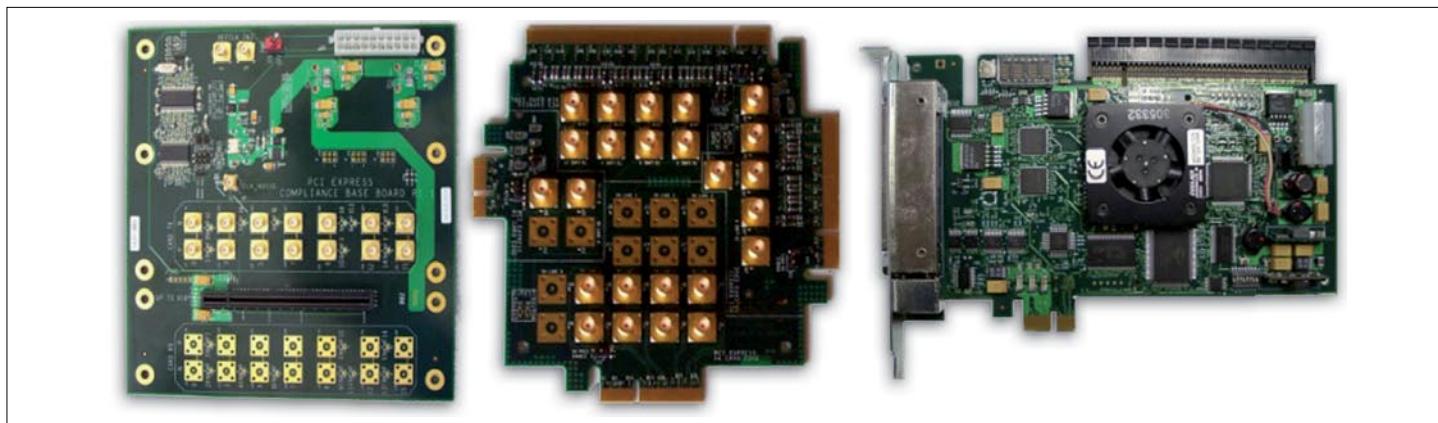


Figure 1: Compliance base board, compliance load board and protocol test card tools are used to validate if PCIe products comply with specifications.

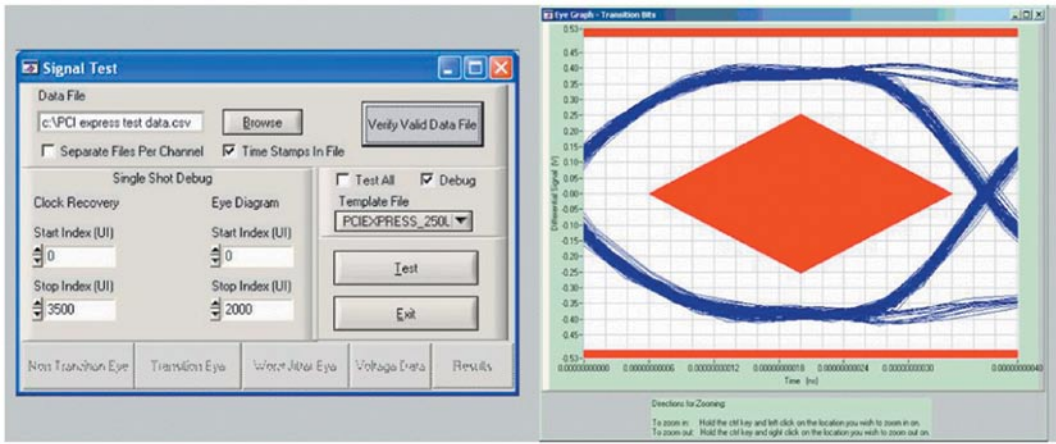


Figure 2: SIGTEST Software, which is provided by PCI-SIG, analyzes the eye pattern, jitter and bit-rate of PCIe components.

When an add-in card arrives at a system suite for interoperability testing, the card is installed and the system is booted into a Windows or Linux environment. Participants verify that the card is detected and configured then they demonstrate the function-

ality of the card. This functionality test is specific to each type of card, but generally consists of basic operations such as file copies, network connectivity or a manufacturer-specific diagnostic routine. Each system and add-in card maintains a test

sheet, which is signed by all participants, showing the pass/fail status of each test in which they participated. At the conclusion of the event, PCI-SIG analyzes the test sheets to determine which products are eligible to be included in the Integrators List.

Another feature of a Compliance Workshop that cannot be realized in-house is the opportunity for engineers to network with colleagues from other companies. Confidentiality is certainly a concern expressed by members. For this, there are processes in place to ensure that unauthorized personnel are not present during test sessions. Moreover, all participants are bound by PCI-SIG confidentiality rules. Despite the presence of unreleased prototypes for testing and various competitors in the same building, the environment is very healthy. Engineers from competing companies help each other. When interoperability tests fail, the participants are willing and able to spend extra time—sometimes beyond normal working hours—and work together to determine the cause of the failure.