Signal integrity issues rise with 500Mbps rates

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Traditionally, chip designers have focused on how to satisfy the functional requirements of devices under time and design rule constraints, but have had no spare time to verify the function in-use-status. Package designers have focused on how to achieve low-cost design under the constraint of electrical, thermal and quality requirements. Only system designers have been conscious of the electrical performance of the system board, such as signal and power integrity, but the electrical model of the device is not always available from LSI suppliers.

SoC designs with data transfer rates beyond 500Mbps fall in a gap between traditional design methods and the proposed chip-package-virtual board co-design method.

This co-design methodology will provide a system solution for cost-sensitive emerging markets by optimizing the electrical and cost requirements. Virtual system simulation could also predict possible electrical problems in advance and reduce the number of sample preparations or repair chances that result in the shorter development lead time.

In the past, the chip, package and board have been designed based on physical information, such as terminal position, I/O count and electrical function for most applications–excluding high-end products. Recent advances in silicon devices have driven increases in chip speed, device density and I/O count, as well as decreases in voltage level toward the SoC.

These advances make the noise and timing budgets tighter, and require applying the method and experience of electrical design considerations developed in the high-end market, such as I/O signal integrity, power integrity and EMI control, in the manner of more systematic design flow to manage larger numbers of design.

The Gbps-level serial interface macro of an SoC is an example of the signal integrity consideration. Since the fine design rule of package interposer is critical for the electrical noise, such as loss, signal reflection and crosstalk, providing an accurate model of the package is indispensable to predict the system response. With the increases in on-chip transistor density and speed, its power level and current have escalated. Including a decoupling design guideline when designing a good power delivery system of the package and board is important to maintain steady power and ground levels during core switching.

Independent designs of chip and package have not resulted in the optimum chip-package and package-board design, and frequent design reconsiderations have lengthened the design lead time. Chip-package co-design could reduce the design lead time and the interposer layer count. One example is a pair of low-voltage differential signals, whose bumps generally stay next to each other. The pair of traces for these bumps needs additional layers for routing to prevent their signals from interfering with each other. Considering the noise budget of chip and package at the same time could help come up with a solution, such as placing ground bumps between a pair of differential clocks, without adding more interposer layers.

Co-design could optimize the fan-out routing from I/O buffer on a chip to the package terminal to minimize the interposer layer count. Package-virtual board co-design could also optimize the layout of package terminals to minimize the layer count of board for signal traces. Developing the co-design methodology of chip-to-motherboard design integration is essential for optimizing the design for performance, cost and design lead-time.

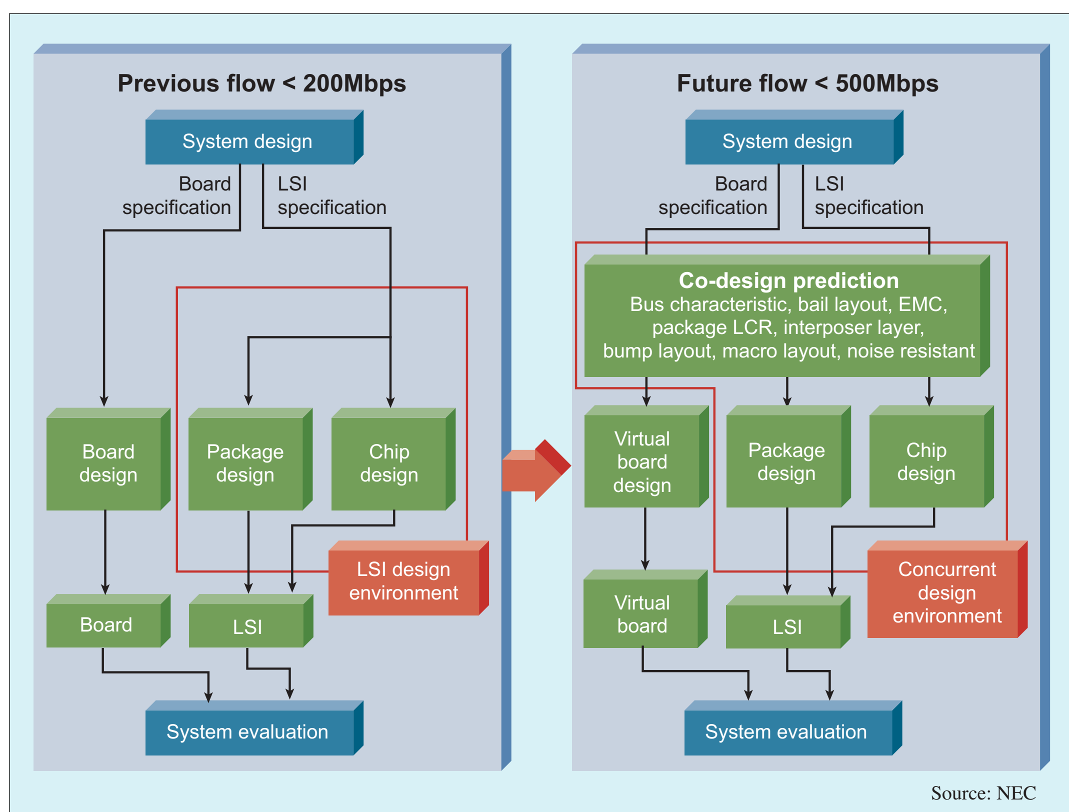
When the data transfer rate of the system is beyond 500Mbps, occasionally the signal, power noise or EMI do not meet the system requirement. In a worst-case scenario, even an SoC device would have to be redesigned as there are no other options but to change the chip and package design. To prevent this, package designers tend to choose an electrically excessive and costly design such as adding extra layers to the already excessive interposer.

To optimize the chip-package-board trade-offs and supply a device at a reasonable cost, engineers have started developing a concurrent design methodology based on the integrated models of the components–chip, package and virtual board–to evaluate signal, power integrity and EMC early in the design procedure.

Interaction gap

Although there are commercially available individual EDA tools for each component, SoC designers have experienced the lack of interaction between these tools or verification of the accuracy of simulated data. Full interaction of each of the component models and verification of the simulated data are the driving force to a balanced design between electrical and cost performance in a short lead-time, which is the final goal of the co-design framework.

The initial stage of SoC de-



Interaction of component models and verification of simulated data drives balance between electrical and cost performance.

sign is selecting the package type and I/O buffer, and designing a rough power delivery based on the design guideline made from the design know-how and some simulation data given by virtual system simulation activity.

After rough designs of the chip and package are made, the network model for a power delivery system on a chip, I/O buffer-, package- and virtual board-model are integrated for the purpose of the system simulation and to obtain assessment of the SoC design in terms of signal integrity, power integrity and EMC. This co-design method is more frequently requested by the customer in a cost-sensitive emerging market, rather than the high-end customer who needs only an accurate model of the chip and package.

The chip-package-board design follows the steps of creating the signal or power model of each component with appropriate mesh size, integrating each model of component for system-level simulation and obtaining feedback to the design parameter of components from the simulated results. These design steps will provide the board design guideline and constraints for high-speed application and an accurate device model for customer use.

Technology development of chip-package-board co-design focuses on two main areas. One area is the modeling technique to integrate the system model to the appropriate data size that still meets the simulation purpose. The other area is co-design framework in conjunction with system simulation and feedback for each design step.

Chip design needs the package and board model as an outside load. Package design needs the I/O buffer model on a chip and board model. Board design needs the package model and I/O buffer model, respectively. For the verification of simultaneous switching output (SSO) noise to the core logic through power traces or through the interposer during I/O buffer design, the package model could be a single load. However, to ensure that SSO noise in the finished product will not cause power level swings and consequently lead to the malfunction of other signals, it is better to use 3D integrated models for the power delivery network to verify the package structure or the I/O buffer design.

Generally, the power delivery network should have sufficiently low impedance, such as negligible IR drop, and enough decoupling capacitance to be resistant to the power- or signal-noise caused by fluctuating voltage levels of the power or ground plane. The estimation of necessary decoupling capacitance and analysis of power noise, such as dynamic IR drop, requires a detailed LRC model for power network on a chip.

Flip-chip and enhanced BGAs are representative of the SoC package and are also both expensive packages, sometimes far more expensive than the chip itself. It is required to design these packages at a low cost such as designing smaller package size, less layer count and inexpensive interposer type.

Even if a designer wanted to redesign the interposer layout based on the simulation results, there would be little room left after the cost-conscious physical design. Electrical budgets are designed ahead of physical design and electrical simulation results are monitored during package design. In the past, the auto-router function of design-CAD was below the expectation of critical package design, but recently developed auto-routers are realizing that expectation. The cooperation between the design-CAD and simulation tool is necessary for both sides.

Since the constraint of model size does not allow for simulating a whole system of chip-package-board, appropriately simplified S-parameter models that describe the electrical characteristics as a parameter of frequency have been used for signal and power integrity.

Multiport preparation

One of the challenges to the power-integrity simulation is to prepare the multiport model, which describes the layout of power and ground balls, under the constraint of data size.

Simple and short signal routings are preferred for all components of chip, package and board to provide better electrical performance and lower cost. Especially in the case of flip-chip BGA packages, the early decision of ball and bump layout are strongly preferred by customers who want to start the board design and by chip designers who also want to start chip design.

A rough floorplanner lays out the I/O buffers and bumps on a chip. Then, an autorouting tool routes the traces from flip-chip-bumps to the reverse side of the interposer, and chooses the best-fit package balls and interposer layer count. The bump pitch, interposer structure and interposer layer count are the major factors of interposer cost. Design rules for these are registered as libraries in the autorouter as a reference for designers who can then select the best combination of these libraries based on the required signal count, performance and cost. A netlist is generated from this step, which can be used to estimate chip performance, designing actual interposer pattern and electrical simulation. □