

Application Notes

Title: ACCEL-to-SPECCTRA Interface and Design Language Translation
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Summary: This application note describes the background involving the interface between ACCEL EDA and Specctra.

When using Specctra, you must translate your design from PCB into a Specctra design file. Any rules that you have set in PCB are translated and embedded in the Specctra design file. So it is always best to add the design rules at the PCB level before interfacing with Specctra. After you finish placing or routing your design, save the Specctra session file or route file. Then, use the translator to return the placement and routing data back to PCB. This is automatically done when using ACCEL EDA to launch Specctra. Please note that in version 14, the ACCEL-to-Specctra interface now supports network licensing. Also, the interface has been updated to include: 1) The Specctra translator detects various new ACCEL PCB design rules, and uses them to automatically produce corresponding Specctra routing rules, 2) The translator also provides more accurate representation of component image outlines. This whole process starts out with the PCB Layout, Intermediate Files, Translator, Design File, Specctra, Session File, Translator, Intermediate Files, and finally back to PCB.

PCB LEVEL

The Specctra design file (.DSN) consists of four basic data types which gets transferred from PCB to Specctra:

- **Design data**, which includes board boundaries, layer definitions, design rules, and keepout definitions.
- **Placement data**, which includes X, Y locations of components and mounting holes on the PCB.
- **Library data**, which includes images for all placed components, and pin and padstack definitions.
- **Network data**, which includes net names, component reference designators, and pin numbers.

Note: The design (.DSN) file produced in PCB always overrides the .DO file produced in Specctra. Do not edit a design file in a text editor. Most translators use the design file to merge the Specctra route data with the original layout system database. If you change the design file and it's no longer synchronized with the layout system database, the translation of route data to your layout system could fail. If you need to make a

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change to the design data, make the change in your layout system and translate the revised design to a Specctra design file.

In PCB, the hierarchical rules are as follows:

- Class-to-Class Rules
- Global Rules
- Layer Sets
- Net Class Definitions
- Net Class Rules
- Net Rules
- Pad Definitions
- Via Definitions

The following attributes are recognized by the autorouter. All other predefined net attributes are ignored for routing.

Attribute	Description
<i>WIDTH</i>	Overrides global line width settings for the selected nets. A line width should be entered as the value.
<i>VIASTYLE</i>	Overrides global via style settings for the selected nets. An existing via style name should be provided.
<i>MAXVIAS</i>	Defines the maximum number of vias that can be placed for this net. Valid values are 0 (no vias) -n (any specific number).
<i>RIPUP</i>	Overrides the global ripup setting for the selected nets. Valid values are No, 0 and False. All indicate that the net should not be ripped up. You can use Yes, 1, and True.
<i>NOAUTOROUTE</i>	Indicates that the selected nets will not be routed. You can use Yes, 1, and True.
<i>AUTOROUTEWIDE</i>	Indicates that the selected nets are scheduled as WIDE passes when you select passes manually. You can use Yes, 1, and True.

PCB DRC verifies clearances and the attributes listed below when they have been defined in the net class:

- MaxNetLength
- MaxVias
- MinNetLength
- ViaStyle

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- Width

For net clearances the rules can be further redefined by specifying clearance rules for pairs of objects, like pad to pad clearances or line to via clearances.

Along with other predefined net attributes, which are available from the **Names** list box, the following clearance attributes are available:

- PADTOPADCLEARANCE
- PADTOLINECLEARANCE
- PADTOVIACLEARANCE
- LINETOLINECLEARANCE
- LINETOVIACLEARANCE
- VIATOVIACLEARANCE
- CLEARANCE

By adding one of these attributes to a net and assigning it a value, the matching global default clearance is overridden for DRC. The value may have a suffix to define the units. If the units are left off, then the current global units are used. If the clearance value can't be converted to a valid number for DRC or autorouting, then the attribute is considered undefined and the corresponding global clearance is used. The last predefined attribute, CLEARANCE, defines a clearance value for all object pairs in this net. For example, if the net-specific clearance between every object pair in a net is the same value, then the CLEARANCE attribute can be used to store that value. This eliminates the need to assign the same value to each of the six clearance attributes.

Below is a small example taken from an actual design (.DSN) file which shows how PCB rules are shown in the Specctra design file:

```
(layer Power
  (type power)
  (use_net VCC)
  (rule (clearance 5 (type pin_pin pin_smd smd_smd)))
  (rule (clearance 5 (type pin_wire smd_wire)))
  (rule (clearance 5 (type wire_wire)))
  (rule (clearance 5 (type smd_via pin_via)))
  (rule (clearance 5 (type via_wire)))
  (rule (clearance 5 (type via_via)))
)
(layer Int2
  (type signal)
  (direction vertical)
  (rule (clearance 5 (type pin_pin pin_smd smd_smd)))
  (rule (clearance 5 (type pin_wire smd_wire)))
  (rule (clearance 5 (type wire_wire)))
  (rule (clearance 5 (type smd_via pin_via)))
  (rule (clearance 5 (type via_wire)))
  (rule (clearance 5 (type via_via)))
)
```

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Specctra does not alter the .DSN file. Only those files which are explicitly written out, such as wires, routes and session (among others), have Specctra modified data contained within them. Even the session (.ses) file needs to have a .DSN file available as a starting point, specifically, the one referred to in the third line of the session file:

```
(session .\power_fanout2.ses
# Session file created by SPECCTRA Version V8.0.3 made 98/11/13 at 15:45:09
(base_design .\power_fanout.dsn)
```

Further rules for controlling routing are through features options. Feature options that are available and supported by the ACCEL-to-Specctra interface are:

- **ADV** (advanced rules)
 - Layer assignment of signals
 - Via assignment by net and net class
 - Width and clearance by layer
 - Net and net class rules by layer
 - Time length factors by layers

- **FST** (fast circuit rules)
 - Crosstalk control by parallelism and accumulated noise rules
 - Timing controls by length or delay
 - Differential pair routing
 - Rules by area
 - Shielding
 - Rounded corners
 - Virtual pin topology control

The following shows a FST example in a .DSN file which routes shields for four nets that will contain t-junctions after routing. To ensure that there is adequate clearance for the shields, the clearance rule for the nets is increased before autorouting. The design is then routed. Because the four nets contain t-junctions, shields are not routed, even though they have a shield rule. Finally, the nets are selected again; their clearance rule is restored; and the shield command is executed to add the shields.

```
select net net1 net2 net3 net4
rule selected (clearance 10)
unselect all
route 25
select net net1 net2 net3 net4
rule selected (clearance 5)
shield
```

SPECCTRA LEVEL

The Specctra .DO file is used to:

- Control Specctra so that the commands in the DO file are read and executed.
- A Do file is an ASCII file that contains sequence of commands.

The Specctra LOG file is a combination of output from the ACCEL-to-Specctra translator, the Specctra autorouter output, and the Specctra-to-ACCEL translator. Postroute processing embeds the status file produced by the auto router into the log file.

When specifying Specctra attributes, this can be done directly in ACCEL PCB by adding the attribute to a net or net class. These attributes are transferred to Specctra through the design file automatically when you click Start on the Autorouters dialog in PCB.

Specctra uses placement rules during both automatic and interactive placement to prevent design rule violations. Placement rules considered at the start of an automatic placement session are:

- Placement grids
- Permitted spacing
- Permitted orientations
- Permitted sides
- Opposite sides

Placement rules set in Specctra override corresponding design file rules.

Specctra rules are also hierarchical. Rules set at one level of the hierarchy take precedence over rules at lower levels. The precedence for all placement rules is (highest to lowest):

- region
- padstack
- class_class_layer
- class_class
- fromto_layer
- fromto
- group_layer
- group
- net_layer
- net

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- group_set_layer
- group_set
- class_layer
- class
- layer
- PCB

PCB placement rules have the lowest precedence in the Specctra rule hierarchy. Rules at this level are observed only if higher precedence rules do not override.

Important ACCEL-to-Specctra Interface Notes:

ACCEL PCB Net Class Rules supported by the Specctra Interface & PCB DRC and used during routing are: Clearance, Width, MaxVias, Max & Min NetLength and Viastyle.

Specctra DO files do not support a layer name that contains a space. If you enter a layer rule for that layer, it will not be recognized correctly since Specctra only looks for the layer name up to the space.

Polygons that are part of a component pattern are not recognized by the interface and may cause shorts. To prevent shorts, place a keepout around pattern polygons.

The Specctra interface does not find PCB files located in the root directory of a hard drive and adds an extra backslash (\) character in the file name so that Specctra cannot find the .DSN file. To fix this, move the PCB file to any subdirectory on the hard drive.

For version 14.0, the following attributes from the Design Rules hierarchy are translated to Specctra routing levels:

- Design Level Width
 BoardEdgeClearance
- Net and Net Class Level Width
 MinNetLength
 MaxNetLength
- Layer Level Width