Translation Of Existing ASIC Designs

ASIC Design Translation

Application Note

Introduction

It has only been in the last few years that designers and users of application specific integrated circuits (ASIC) have been able to obtain additional sources for these types of integrated circuits. The introduction of design synthesis software by CAD / CAE companies has made the task of converting from one ASIC vendor's library into another's, a feasible task even for the most dense designs.

The user of an application specific integrated circuit who desires the flexibility and security offered by having multiple sources for what are often key system components, or the user who requires an improvement in performance offered by advanced process technologies, now have an easy path to satisfy their needs. That path is Atmel's Design Translation ASIC design flow, shown in Figure 1. The Design Translation flow highlights the major steps that are taken in converting a netlist into Atmel's gate array cells, verifying the translation, performing the layout and realizing the desired circuit performance, and fabricating and testing the resulting silicon product.

This application note describes the types of data required from the ASIC user and the process steps followed by Atmel to successfully translate an existing ASIC design, and presents the results of two translation efforts. The first was an effort where the Atmel device performance was required to match that of the original ASIC. The second was a translation where the improved performance of Atmel's device was required. The process has been proven through successful translation of designs from such vendors as LSI Logic, NEC, Fujitsu, and Oki, into our 1.0 µ ATL series gate array family.

The Process

Simply stated, the Design Translation process maps cells from the original design into cells contained in Atmel's cell library. These cells may be equivalent primitives or may be soft macros which include several primitives. The choice of Atmel cell will depend upon the required performance objective, and, in some instances, hard macros may be created to replace soft macros to achieve performance goals for the design.

Once the mapping is complete, the process follows Atmel's normal ASIC design flow, including cell placement and routing, resimulation using Atmel's "golden" simulator, comparison of predicted versus desired performance and, after approval of the design by the user, PG tape out and prototype fabrication.

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Database Required

ASIC design can be accomplished on a variety of platforms, and with a variety of software tools - some open, some proprietary. Designs are completed using generic and/or vendor-specific library cells as well. This level of flexibility available to the ASIC designer does not hinder the translation effort. Most design tools are capable of providing a netlist in EDIF (EDIF 2.0.0) format. Other netlist formats which are acceptable to Atmel are listed below:

- Cadence™ - Verilog-XL™ , EDIF 2.0.0
- LSI Logic - NDL™
- Mentor™ - MIF™
- Synopsys™ - db, EDIF
- Viewlogic™ - EDIF 2.0.0

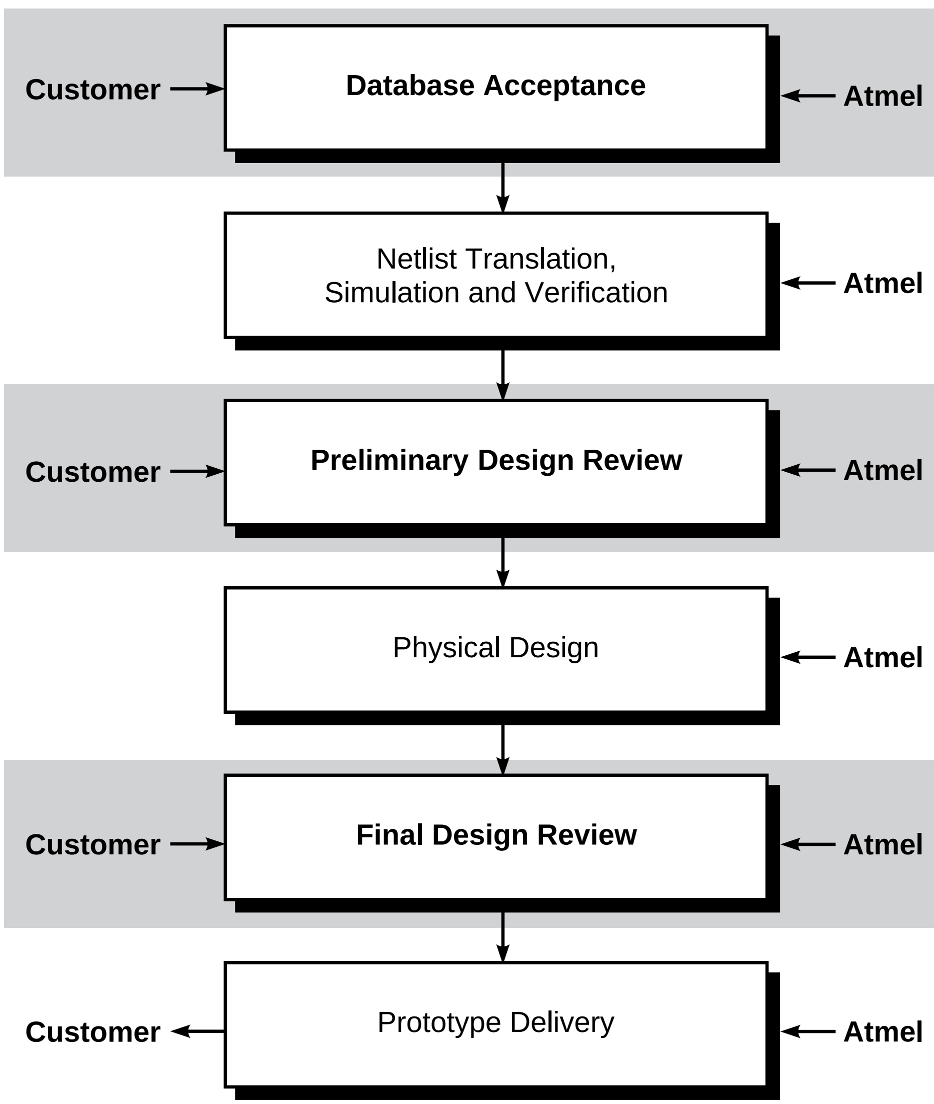
In addition to the netlist for the original design, several other pieces of information are needed to successfully translate the design. Also required are:

- A description of the original design library
- Functional test vectors, print-on-change format
- Device specifications
- Identification of critical and/or asynchronous paths

"As-routed" delay data from the original design

To make an assessment of whether the desired performance match or improvement has been achieved, an understanding of the starting point must be reached. The description of the original cell library, with its functional and timing information for each cell, is also essential to the definition of the starting point.

Figure 1. Design Translation Flow



If sample parts of the original design can be provided, performance data on the actual silicon can be used to help establish a baseline.

The functional vector set (in ASCII or TSSI, print-on-change format) serves two purposes. The functional vector set, when converted into tester-specific format and used in conjunction with the sample devices, provides a mechanism for establishing detailed performance attributes of the original design. These attributes, such as maximum frequency, path timing performance, and buffer characteristics to name a few, provide the base for cell and buffer selection to match or improve the design. Individual performance attributes can also be used as input to a waveform comparison tool. This tool, using the actual data and the functional test vectors, now converted to simulator format, permits the Atmel designer to determine when and where timing mismatches occur and adjust the netlist accordingly.

The device specification provides key information concerning the required device pin-out, system loading for each pin, the desired performance, and the range of operating conditions.

Performance Matching

Our first example of ASIC translation presents the results of work performed for a military application, where interchangeability with the original designs was required. The original design was an LSI Logic 10K series gate array of approximately 5,000 gates. The design was asynchronous and had multiple clocks. Samples representing the original designs were available at the outset and were characterized to supplement the specification requirements. All the data presented is a direct comparison of LSI Logic and Atmel silicon. Figure 2, depicting maximum operating frequency for constant temperature and voltage, shows how closely the performance can be matched. Figures 3 and 4 depict the average performance for nine critical paths, for low-to-high transitions, both as a function of supply voltage and of temperature. And finally, Figures 5 and 6 depict rise and fall time of bidirectional buffers. The performance match is extremely close.

The customer performed extensive tester-based characterization and qualification of the Atmel device to insure that it was pin-for-pin compatible, drop-in

Figure 2. Maximum Operating Frequency, 25°C, V_{DD}=5.0V

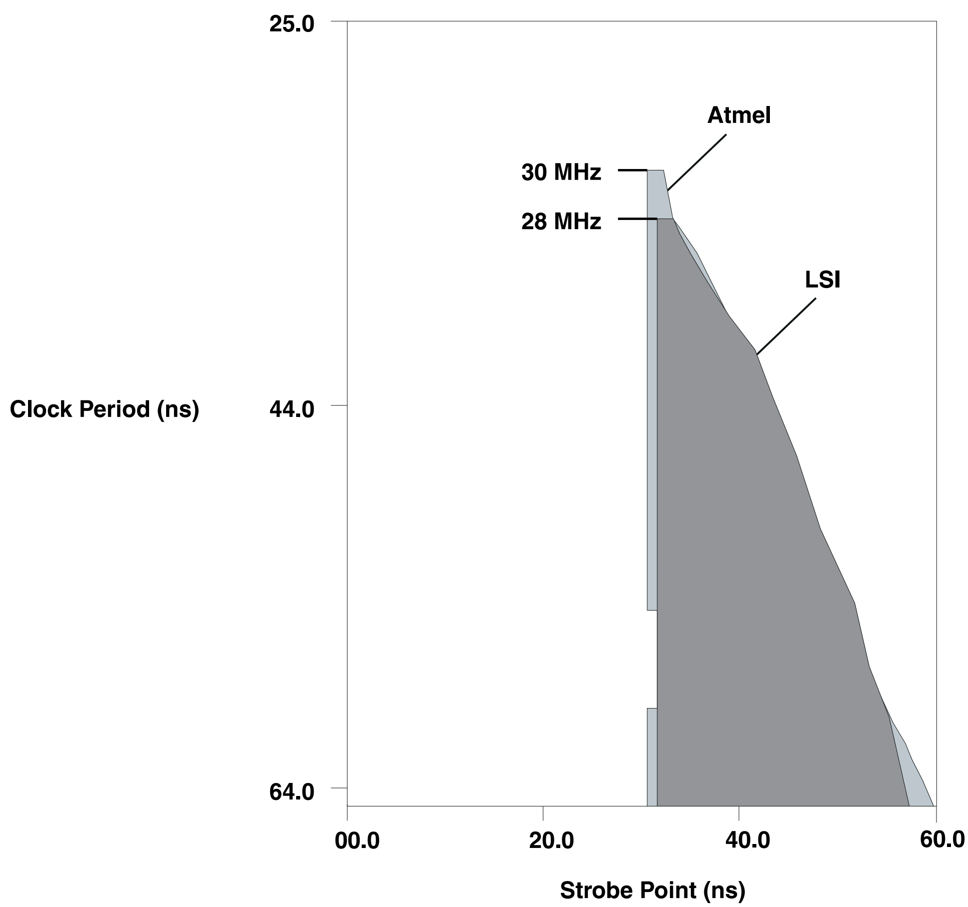


Figure 3. Atmel vs LSI Package Test Results for 9 Critical Paths, t_{PLH}, +25°C

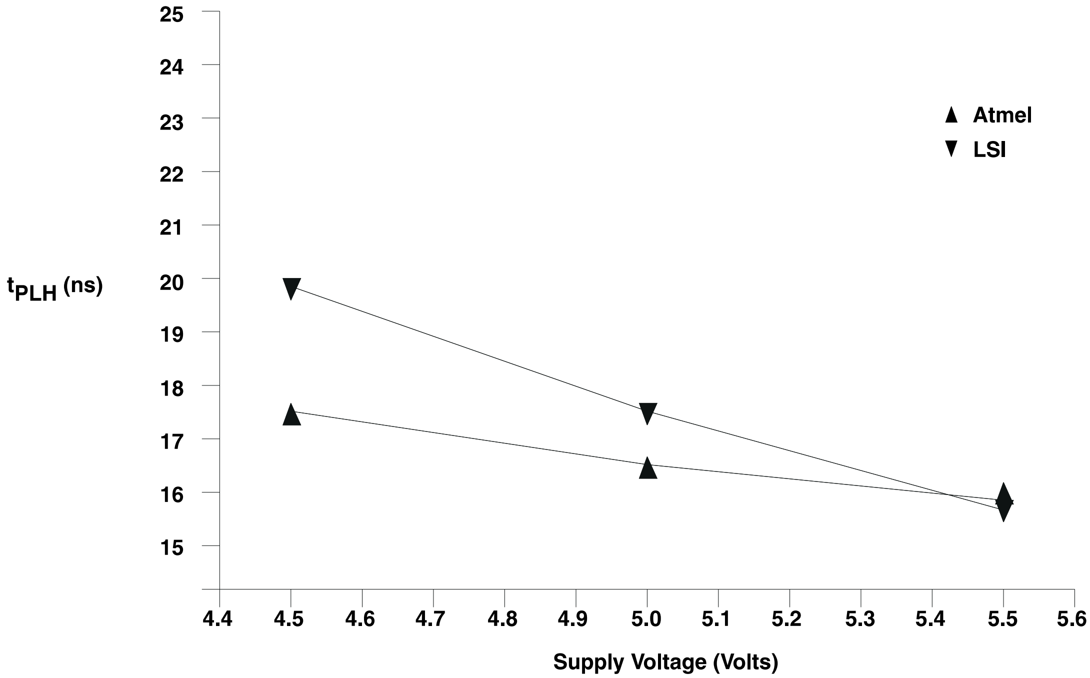
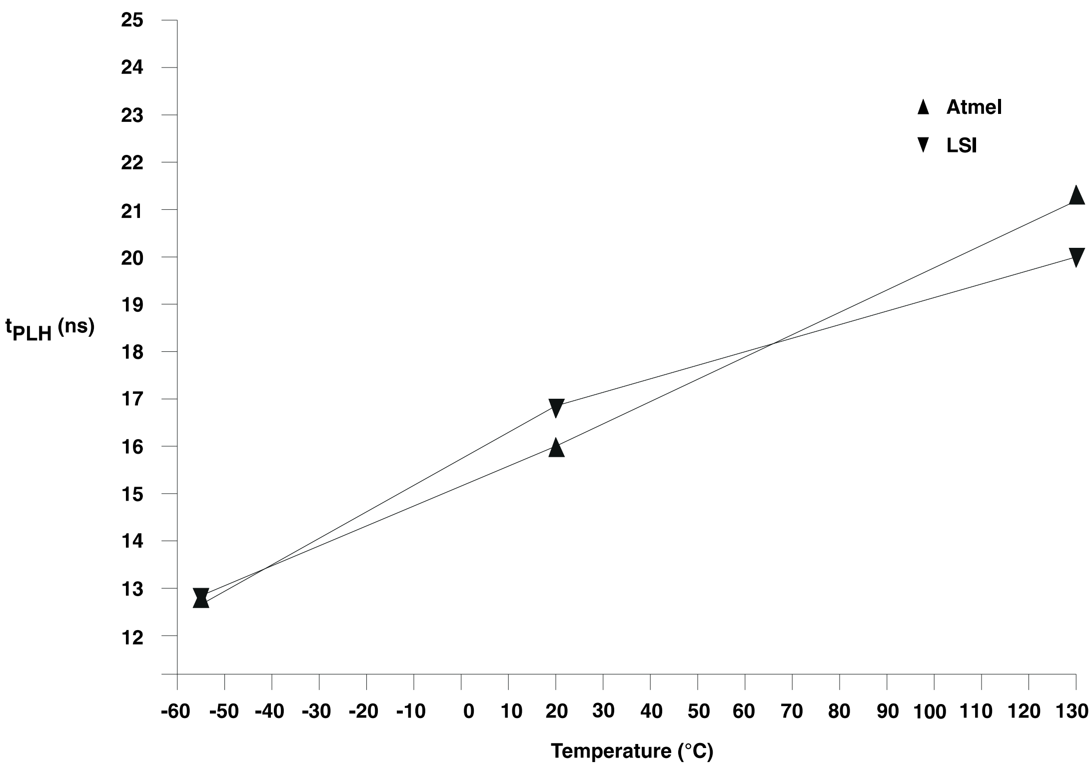


Figure 4. Atmel vs LSI Package Test Results for 9 Critical Paths, t_{PLH}, V_{DD} = 5.0 V



replacement of the original LSI Logic part. The parts were then assembled onto boards and tested again. The Atmel and LSI parts were interchanged and mixed and matched on boards. The complete system evaluation was performed and in all tests the Atmel parts proved to be equal or superior to the LSI gate array.

Figure 5. Output Rise Time, 8 mA Bidirectional Buffer, 25°C, 120 pF Load, V_{DD} = 5.0 V

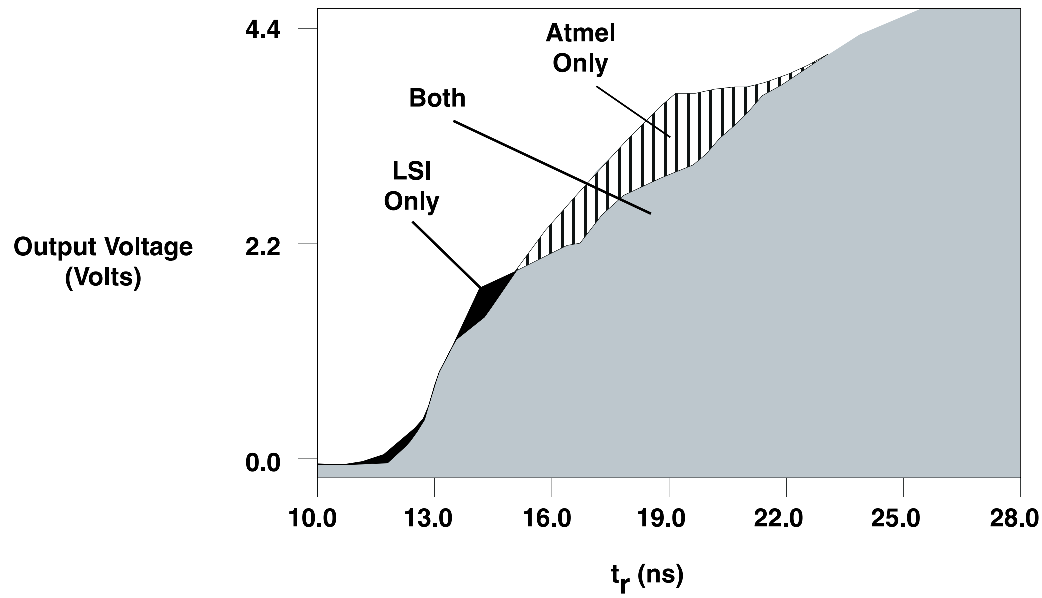
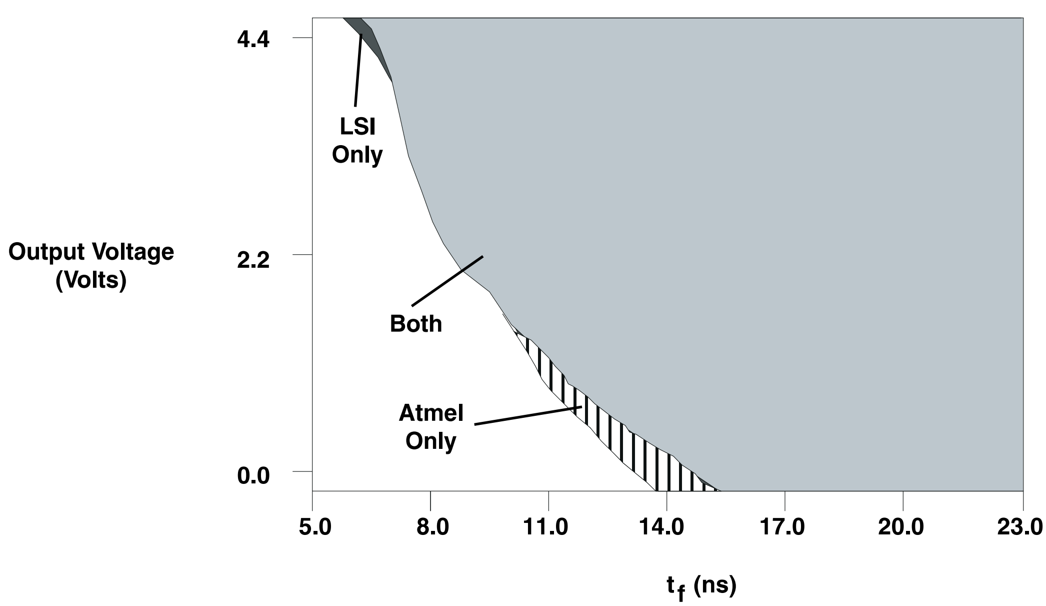


Figure 6. Output Fall Time, 6 mA Bidirectional Buffer 25°C, 120 pF Load, V_{DD} = 5.0 V



Performance Improvement

The second example of ASIC translation presents the results of work performed for a commercial application. This design required approximately 8,000 gates, was completely synchronous, and was operating at 25 MHz. The customer desired an improvement in performance to 33 MHz. To achieve this speed, Atmel compared the performance of its cells to those of the original design, as samples were not available. This evaluation indicated that a 30 to 35 percent speed improvement could be realized over the existing design. Atmel also employed higher drive cells where appropriate to further enhance performance.

Extensive board level testing, performed by the customer, confirmed that the Atmel implementation exceeded the 33 MHz design goal over the rated voltage and temperature ranges.

Atmel's CMOS Gate Array Design Manual provides more detailed information about the gate arrays, design methodologies, and individual cell timing, and should be used as a reference for evaluating ASIC performance.